PROGRAMMABLE HIGH-FREQUENCY CRYSTAL OSCILLATOR

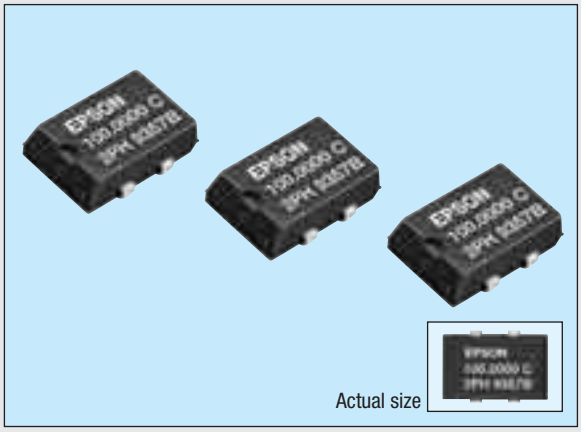
SG-8002JA series

Product number (please refer to page 2)

Q3306JAxxxxxx00

- Wide frequency output by PLL technology.
- Quick delivery of samples and short lead mass production time.
- Excellent environmental capability.
- Output enable function (OE) and stand-by function ($\overline{ST}$) can be used for low current consumption applications.
- Package and pin compatible with SG-615.
- Available for lead (Pb)-free soldering.
- Available for lead (Pb)-free terminal.

SG-Writer available to purchase.
Please contact EPSON or local sales representative.



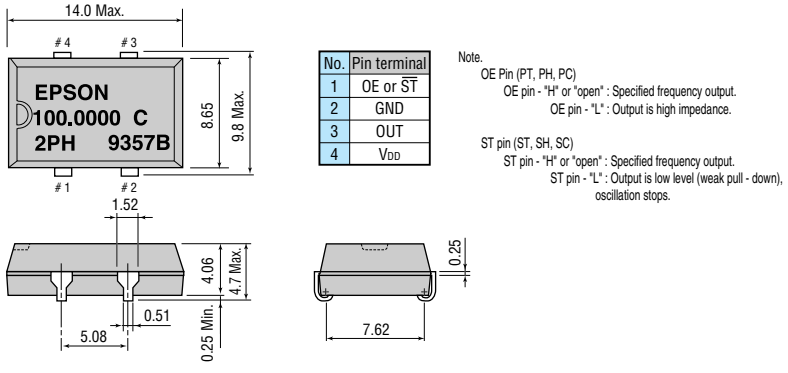
■ Specifications (characteristics)

Item		Symbol	Specifications *2			Remarks
			PT / ST	PH / SH	PC / SC	
Output frequency range		fo	1.0000 MHz to 125.0000 MHz			Refer to page 50. "Frequency range"
Power source voltage	Max. supply voltage	VDD-GND	-0.5 V to +7.0 V			
	Operating voltage	VDD	5.0 V ±0.5 V		3.3 ± 0.3 V	2.7 V to 3.6 V : fo ≤ 66.7 MHz (PC / SC)
Temperature range	Storage temperature	TSTG	-55 °C to +125 °C			Stored as bare product after unpacking
	Operating temperature	TOPR	-20 °C to +70 °C (-40 °C to +85 °C)		-40 °C to +85 °C	Refer to page 50. "Frequency range"
Frequency stability		Δf/fo	B: ±50 x 10^{-6} C: ± 100 x 10^{-6}			B, C : -20 °C to +70 °C
			M: ±100 x 10^{-6}			M : -40 °C to +85 °C
Current consumption		IOP	45 mA Max.		28 mA Max.	No load condition, Max. frequency range
Output disable current		IOE	30 mA Max.		16 mA Max.	OE = GND (PT, PH, PC)
Standby current		IST	50 µA Max.			$\overline{ST}$ = GND ($\overline{ST}$, SH, SC)
Duty *1		tw/ t	–	40 % to 60 %		CMOS load: 1/2 VDD level
			40 % to 60 %	–		TTL load: 1.4 V level
High output voltage		VOH	VDD -0.4 V Min.			IOH = -16 mA (PT / ST, PH / SH),-8 mA (PC / SC)
Low output voltage		VOL	0.4 V Max.			IOL = 16 mA (PT / ST, PH / SH), 8 mA (PC / SC)
Output load condition (fan out) *1	TTL	N	5 TTL Max.	–		Max. frequency and Max. operating voltage range
	CMOS	CL	15 pF Max.	25 pF Max.	15 pF Max.	
Output enable / disable input voltage		VIH	2.0 V Min.		0.7 VDD Min.	$\overline{ST}$, OE terminal
		VIL	0.8 V Max.		0.2 VDD Max.	
Output rise time *1	CMOS level	tR	–	4 ns Max.		CMOS load: 20 % → 80 % VDD
	TTL level		4 ns Max.	–		TTL load: 0.4 V → 2.4 V
Output fall time *1	CMOS level	tF	–	4 ns Max.		CMOS load: 80 % → 20 % VDD
	TTL level		4 ns Max.	–		TTL load: 2.4 V → 0.4 V
Oscillation start up time		tOSC	10 ms Max.			Time at minimum operating voltage to be 0 s
Aging		fa	±5 x 10^{-6} / year Max.			Ta = +25 °C, VDD = 5.0 V / 3.3 V, First year
Shock resistance		S.R.	±20 x 10^{-6} Max.			Three drops on a hard board from 750 mm or excitation test with 29400 m/s² x 0.3 ms x 1/2sine wave in 3 directions

*1 Operating temperature (-40 °C to +85 °C), the available frequency, duty and output load conditions, please refer to page 50, 51.
*2 PLL - PLL connection & Jitter specification, please refer to page 52.
Checking possible by the Frequency Checking Program. http://www.epsondevice.com/domcfg.nsf

■ External dimensions

(Unit: mm)



No.	Pin terminal
1	OE or $\overline{ST}$
2	GND
3	OUT
4	VDD

Note.
OE Pin (PT, PH, PC)
OE pin - "H" or "open" : Specified frequency output.
OE pin - "L" : Output is high impedance.

ST pin (ST, SH, SC)
ST pin - "H" or "open" : Specified frequency output.
ST pin - "L" : Output is low level (weak pull - down), oscillation stops.

■ Recommended soldering pattern

(Unit: mm)