Complex Programmable Logic Device

ATF15xx In-System Programming

USER GUIDE

Introduction

The Atmel® ATF15xx Complex Programmable Logic Devices (CPLDs) with Logic Doubling® architecture support In-System Programming (ISP) through the IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface. This feature enhances programming flexibility and provides benefits in various phases; product development, production, and field use. This user guide describes the design methods and requirements for implementing ISP on ATF15xx CPLDs with ISP support as listed below:

- ATF1502AS/ASL/ASV
- ATF1504AS/ASL/ASV/ASVL
- ATF1508AS/ASL/ASV/ASVL

Features and Benefits

In-system programming allows the programming and re-programming of ISP devices after they are mounted onto the Printed Circuit Boards (PCBs). This eliminates the extra handling step required in the manufacturing process to program the devices on an external device programmer before they are mounted on the PCBs. Eliminating this step reduces the possibility of damaging the delicate leads of high pin count surface mount devices or damaging the device through electrostatic discharge (ESD) during the programming flow. ISP also allows users to make design changes and field upgrades without having to remove the ISP devices from the PCBs. Furthermore, it also allows the use of an embedded microcontroller or in-circuit tester to perform in-system programming operations on the ISP devices and integrate these programming operations into the production flow of the circuit boards.

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1. In-System Programming Systems

The three essential components of an ISP system for the ATF15xx CPLDs are:

Software	Implementation of the programming algorithm, as well as the generation of the JTAG instructions and data for the target ISP devices. This can be a software program running on a PC, an embedded microcontroller, or an in-circuit testing equipment.
Interface Hardware	Communication channel between the ISP software and ISP devices on the target board. This can be an ISP download cable or programmer from Atmel or a third-party vendor, an in-circuit testing equipment, or the connections between an embedded microcontroller and ISP devices on the PCB.
Target Board	Circuit board containing the ISP devices in the JTAG chain. This can be the ATF15xx CPLD Development/Programmer board from Atmel or a custom designed circuit board with the appropriate JTAG connections to the interface hardware.

In addition to these three components, a JEDEC file is necessary to program an ATF15xx CPLD. This JEDEC file can be created by compiling a design file using development software that supports the ATF15xx CPLDs such as Atmel WinCUPL and Atmel ProChip Designer. Atmel also provides a translator software utility, POF2JED.exe, that converts output file from the competitor's programming format to a JEDEC file compatible with the ATF15xx CPLD. For more information on this utility, please refer to the Atmel application note, "ATF15xx Product Family Conversion", available on the Atmel website. After the JEDEC files are created for all ATF15xx CPLDs, they can be programmed on the target board.

The ATF15xx CPLDs can be programmed by the following in-system programming systems:

- ATF15xx In-System Programming system
- Embedded microcontrollers
- In-circuit testers

1.1. Atmel ATF15xx In-System Programming System

For in-system programming of the ATF15xx CPLDs, ISP software, download cable, and development/programmer kit are available from Atmel and they are described in the sections below.

1.1.1. ISP Software

The Atmel ATF15xx ISP software, ATMISP, is the primary means for implementing JTAG in-system programming on the ATF15xx CPLDs. ATMISP runs on a Windows based host PC and implements in-system programming of the ATF15xx CPLDs on the target ISP hardware system or generates a Serial Vector Format (.SVF) file to be used by Automatic Testing Equipment (ATE) to program the ATF15xx CPLDs on the target system. ATMISP first acquires all the necessary information from the users about the JTAG device chain in the target system. It then executes the appropriate JTAG ISP instructions onto the JTAG device chain in the target system according to the JTAG device chain information specified by the users through the PC's USB or LPT port. More information about the Atmel ATMISP software is available at www.atmel.com/tools/ATMISP.aspx.

1.1.2. ISP Download Cable

The Atmel ATF15xx USB-based ISP Download Cable, ATDH1150USB, connects to a standard USB port of a host computer on one side and to a JTAG header of the target circuit board on the other side. It transfers the JTAG instructions and data generated by ATMISP running on the host PC to the ISP devices on the target circuit board. More information about the ATDH1150USB cable is available at www.atmel.com/tools/ATDH1150USB.aspx.

1.1.3. Development/Programmer Kit

The Atmel ATF15xx Development/Programmer Kit, ATF15xx-DK3-U, is a complete development system and an ISP programmer for the ATF15xx CPLDs. This kit provides designers a very quick and easy way to develop prototypes and evaluate new designs with an ATF15xx ISP CPLD. With the availability of the different socket adapter boards to support most of the package types offered in the ATF15xx CPLDs, this kit can be used as an ISP programmer to program the ATF15xx ISP CPLDs in most of the available package types through the JTAG interface. More information about the Atmel ATF15xx-DK3-U kit is available at www.atmel.com/tools/ATF15XX-DK3-U.aspx.

1.2. Embedded Microcontroller System

The programming algorithm and JTAG instructions for the ATF15xx CPLDs can be implemented in a microcontroller or microprocessor, which can then be used to program the ATF15xx CPLDs on the target board. One possible method is to extract all the pertinent JTAG protocol information (i.e. JTAG instructions and data) from the SVF file generated by the ATMISP software, and then use this information to implement code for the microcontroller or microprocessor that would generate the JTAG signals for the ISP devices in the JTAG chain. This approach is most suitable for systems that already have an embedded microcontroller or microprocessor, and this eliminates the use of external in-system programming software and hardware tools.

1.3. In-circuit Testing System

The ATF15xx CPLDs can be programmed on the target circuit board via the JTAG interface during the testing of the circuit board using an in-circuit tester. Generally, the SVF file generated by ATMISP should contain all of the pertinent JTAG in-system programming information that the in-circuit testers need to program the ATF15xx CPLDs on the target circuit board. This approach allows the integration of the programming step into the testing stage of the production flow.

2. JTAG ISP Interface

ISP for the ATF15xx CPLDs is implemented using the IEEE 1149.1 Std. JTAG interface. This interface can be used to erase, program, and verify the ATF15xx CPLDs. The JTAG interface is a serial interface consisting of the TCK, TMS, TDI, and TDO signals and a JTAG Test Access Port (TAP) controller. The TCK pin is the clock input for the JTAG TAP controller and to shift in/out the JTAG instructions and data. The TDI pin is the serial data input. It is used to shift programming instructions and data into the ISP devices. The TDO pin is the serial data output. It is used to shift out data from the ISP devices. The TMS pin is a mode select pin. It controls the state of the JTAG TAP controller.

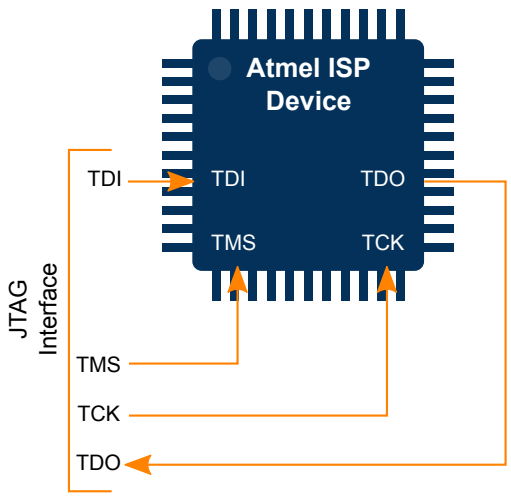
The JTAG interface pins of the ATF15xx CPLD on the ISP target board must be connected to the ISP interface hardware (i.e. ISP download cable) typically via a 10-pin header. The ISP interface hardware also needs to be connected to the host PC running the ISP software. The ISP interface hardware establishes communication between the ISP software and ISP devices, and it allows the ISP software to transfer the programming instructions and data from the host PC to the ATF15xx CPLDs.

ATF15xx CPLDs with the JTAG feature enabled are fully JTAG compatible and also support the required Boundary Scan Test (BST) operations specified in the JTAG standard. The ATF15xx CPLDs can be configured to be part of a JTAG BST chain with other JTAG devices for in-circuit testing of the system board. With this feature, the ATF15xx CPLDs can be tested on the circuit board along with other JTAG supported devices without resorting to bed-of-nails testing.

2.1. Single Device Programming

The JTAG ISP interface can be configured to program a single ATF15xx CPLD. The JTAG configuration for a single device is shown in the figure below. When an ATF15xx CPLD is configured in this way, a register appears between the TDI and TDO pins of the device. The size of the register depends on the JTAG instruction width and the data being shifted in for that instruction.

Figure 2-1 JTAG Device

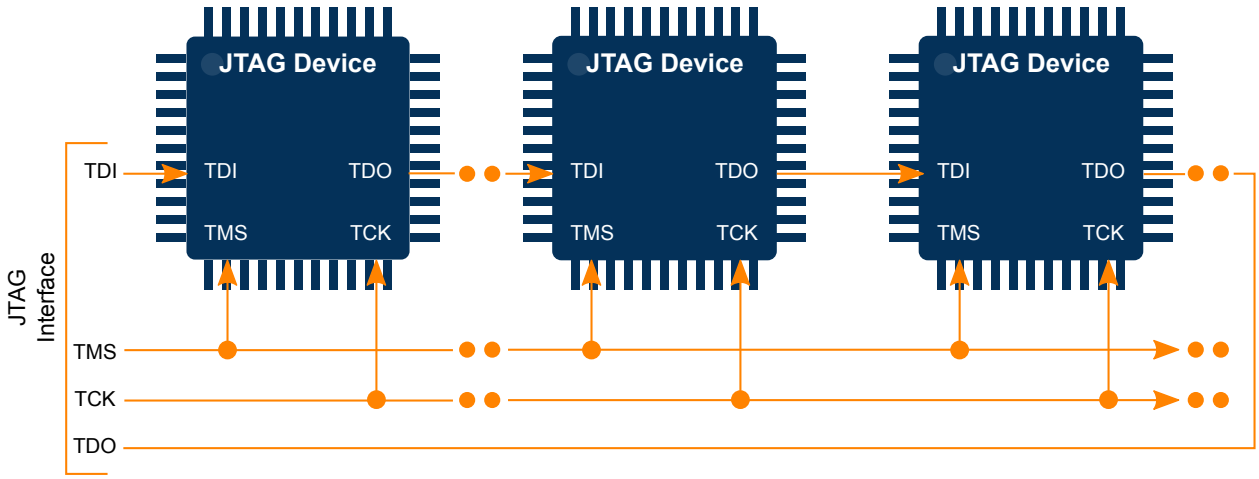


2.2. Multiple Device Programming

The ATF15xx CPLDs can be configured as part of a daisy chain of multiple JTAG supported devices as described below and also shown in the following figure.

1. Connect the TMS and TCK pin for each device in the JTAG chain to the TMS and TCK pins of the JTAG interface header on the circuit board.
2. Connect the TDI pin from the first device to the TDI pin of the JTAG interface header.
3. Connect the TDO pin from first device to the TDI pin of the next device. Continue this process until all except the last one are connected.
4. Connect the TDO pin from the last device to the TDO pin of the JTAG interface header.

Figure 2-2 Multiple Device JTAG Configuration



To program multiple devices in a JTAG chain, users must use ISP software tools that support such feature. In the ISP software, users need to specify:

- Number of devices in the JTAG chain.
- Part numbers of the devices and the positions within the JTAG chain.
- JTAG operations for each of the devices.
- Other JTAG related information such as the JTAG instruction width for each of the devices.

Once the JTAG daisy chain is properly setup on the ISP target board and in the ISP software, the devices in the JTAG chain can be programmed at the same time.

3. Design Considerations

To perform ISP on an ATF15xx CPLD, resources for the JTAG interface in the ATF15xx must be reserved. Therefore, the four I/O pins for the TMS, TDI, TDO, and TCK pins must be reserved for JTAG and cannot be used as user I/Os. The pin numbers for these pins depend on which ATF15xx CPLD is used and its package type. Refer to the table below for pinout information. The JTAG standard recommends that the TMS and TDI pins be pulled up for each device in the JTAG chain. The ATF15xx CPLDs have an internal pull-up feature for these pins which, when enabled, saves the need for external pull-up resistors.

Furthermore, the JTAG interface feature must be enabled in order to perform ISP on the ATF15xx CPLDs. Enabling the JTAG interface requires choosing specific Atmel device types or option setting before compiling the ATF15xx design. These procedures are outlined for WinCUPL, ProChip Designer, and POF2JED in this guide. By default, all brand new ATF15xx CPLDs are shipped with the JTAG interface enabled.

Once logic resources for the JTAG interface are reserved, users can program, verify, and erase any ATF15xx CPLD on the target board using the ATMISP software.

Tip:
Although the four JTAG pins are reserved for a JTAG interface, users can implement buried logic functions in the macrocells associated with these pins.

Table 3-1 ATF15xx CPLD JTAG Pin Numbers

JTAG Pin	44-TQFP	44-PLCC	84-PLCC	100-TQFP	100-PQFP
TDI	1	7	14	4	6
TDO	32	38	71	73	75
TMS	7	13	23	15	17
TCK	26	32	62	62	64

3.1. Enable JTAG Interface with WinCUPL

To enable the JTAG interface with WinCUPL, the appropriate ATF15xx ISP device type needs to be specified before a design is compiled. After a design is successfully compiled, a JEDEC file with the JTAG interface feature enabled is generated. When this JEDEC file is programmed into an ATF15xx CPLD, its JTAG interface is enabled.

Users can also enable the TDI and TMS internal pull-up resistors by including the following property statements in the CUPL design file.

```
PROPERTY ATMEL {TDI_PULLUP = ON};
```

```
PROPERTY ATMEL {TMS_PULLUP = ON};
```

Notice:
If an ATF15xx ISP device type is used for a design that uses the JTAG interface pins as logic I/O pins, WinCUPL generates an error.

The following steps discuss how to open an existing design in WinCUPL, specify the device type, and compile the design.

1. On the WinCUPL main menu, select ***File*** > ***Open***. Select the CUPL (.pld) source file from the appropriate working directory.
2. Select ***OK*** to open the PLD source file.
3. On the WinCUPL main menu, select ***File*** > **Save**. This saves changes made to the source file.
4. On the main menu, select ***Options*** > ***Devices***. This opens the ***Device Selection*** dialog box.
5. Choose the appropriate ATF15xx ISP device. See the following table for a listing of all the ATF15xx device types supported by WinCUPL.
6. Select ***OK*** to close the device selection menu.
   Note: An alternate method is to choose an appropriate ATF15xx device type from the following table and include it in the header section of the CUPL source file.
7. On the WinCUPL main menu, select ***Run***> ***Device Dependent Compile***.
   - WinCUPL compiles the design and spawn the Atmel device fitter. If the design fits, a JEDEC file is automatically created.
   - When the JEDEC file is programmed into the device, the JTAG interface, the optional internal TMS and TDI pull-ups, and the optional pin-keeper circuits are enabled.

   Note: Selecting an Atmel ISP device type automatically enables the JTAG interface by default when Atmel WinCUPL runs the Atmel device fitter.

If the designs prevent reserving resources for the JTAG interface or an ISP is optionally not used, an Atmel non-ISP device type must be selected. See the table below for a listing of devices. The device can then be reprogrammed using an external device programmer.

The below table lists the Atmel ISP and Atmel non-ISP device types for WinCUPL.

Table 3-2 WinCUPL ATF15xx Device Type

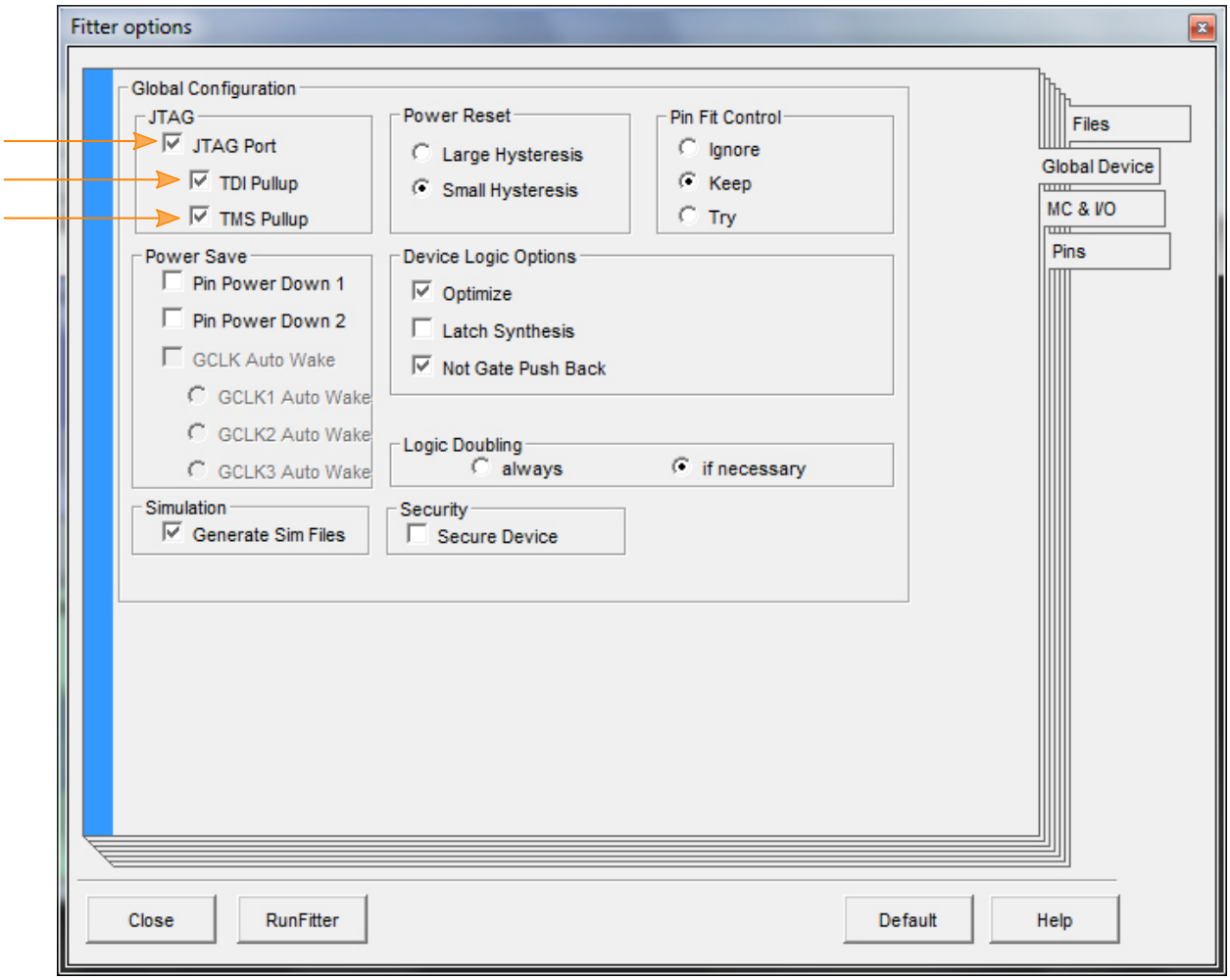
Device Name	Package Type	WinCUPL Device Type	
		JTAG Enabled	JTAG Disabled
ATF1502AS/ASL/ASV	PLCC44	F1502ISPPLCC44	F1502PLCC44
ATF1502AS/ASL/ASV	TQFP44	F1502ISPTQFP44	F1502TQFP44
ATF1504AS/ASL/ASV/ASVL	PLCC44	F1504ISPPLCC44	F1504PLCC44
ATF1504AS/ASL/ASV/ASVL	TQFP44	F1504ISPTQFP44	F1504TQFP44
ATF1504AS/ASL/ASV/ASVL	PLCC84	F1504ISPPLCC84	F1504PLCC84
ATF1504AS/ASL/ASV/ASVL	TQFP100	F1504ISPTQFP100	F1504TQFP100
ATF1508AS/ASL/ASV/ASVL	PLCC84	F1508ISPPLCC84	F1508PLCC84
ATF1508AS/ASL/ASV/ASVL	TQFP100	F1508ISPTQFP100	F1508TQFP100
ATF1508AS/ASL/ASV/ASVL	PQFP100	F1508ISPQFP100	F1508QFP100

3.2. Enable JTAG Interface with Atmel ProChip Designer

To enable the JTAG interface with ProChip Designer:

1. Open the appropriate ProChip Designer project.
2. Open the Fitter Options window by clicking on the ***Atmel Fitter*** button under ***Device Fitter***.
3. Select the ***Global Device*** tab and then check the ***JTAG Port*** box. The TMS and TDI internal pull-up resistors can also be enabled by checking the ***TDI Pullup*** and ***TMS Pullup*** boxes. These check boxes are shown in the figure below.

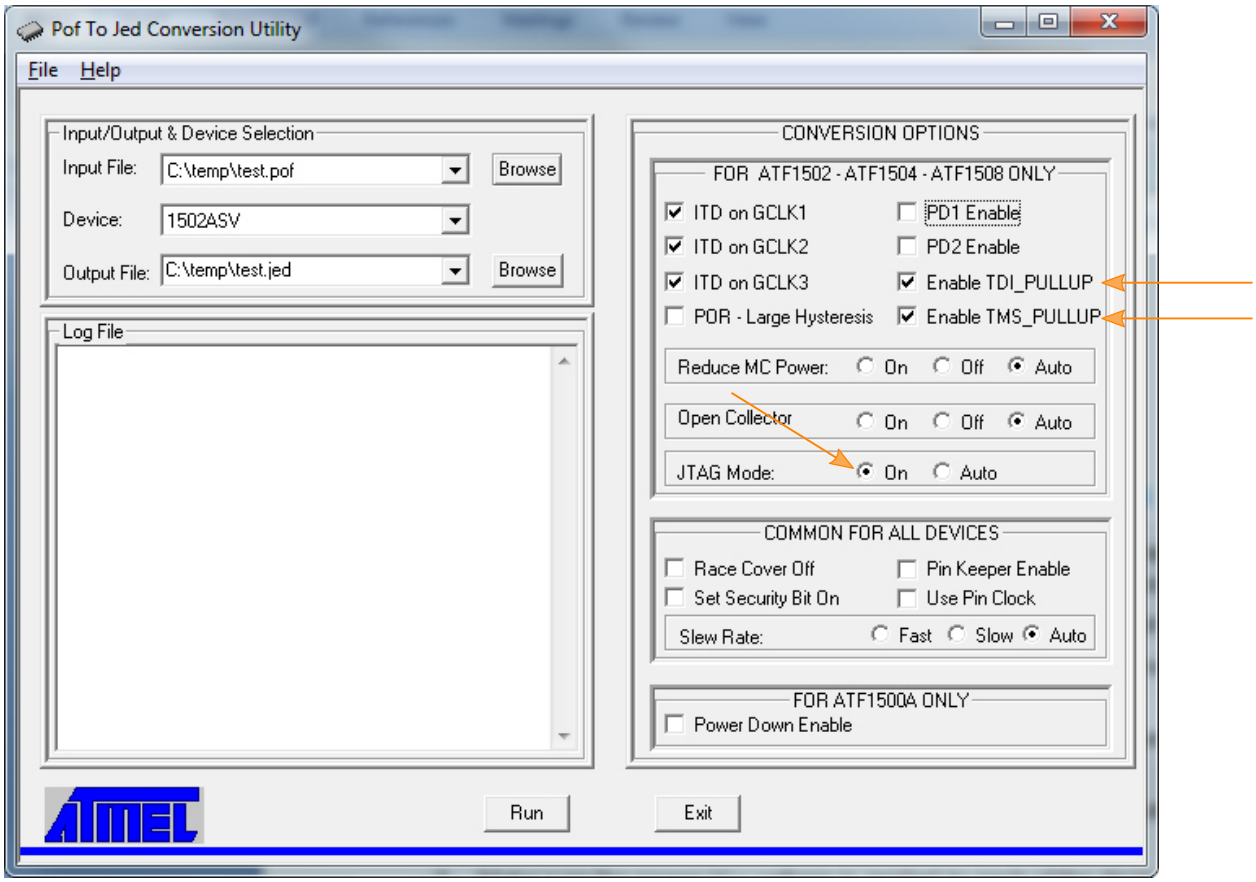
Figure 3-1 ProChip Designer Fitter Options User Interface



3.3. Enable JTAG Interface with POF2JED

In POF2JED, the ***JTAG Mode*** option can be set to ***Auto*** to let POF2JED determine whether the JTAG feature in the ATF15xx should be enabled or not, and it is based on whether JTAG is supported in the competitor's CPLD. To turn on JTAG in the ATF15xx CPLD regardless of whether JTAG is supported in the competitor's CPLD or not, the ***JTAG Mode*** option should be set to ***On***. When JTAG is enabled in the ATF15xx, the TDI and TMS internal pull-up resistors can be enabled by checking the ***Enable TDI_PULLUP*** and ***Enable TMS_PULLUP*** boxes in POF2JED. See the figure below.

Figure 3-2 POF2JED User Interface



4. Guidelines and Recommendations

Attention:
Extra attention to this section should be made when performing ISP operations on ATF15xx CPLDs. This section discusses some of the JTAG ISP guidelines, information and recommendations that should be well noted.

1. Make sure the JTAG port for all of the devices in the JTAG chain are enabled.
   - For the ATF15xx CPLDs, the JTAG port is enabled if the devices are blank/erased or programmed with JTAG enabled.
   - All Atmel ATF15xx devices are shipped in the blank/erased state; therefore, the JTAG port is enabled for all brand new devices and ready for ISP.
   - ATF15xx devices with JTAG disabled need to be erased using a non-ISP device programmer to re-enable the JTAG port.
2. Make sure the proper V_{CC} voltage is applied to each of the devices in the JTAG chain.
   - ATF15xxAS/ASL CPLDs in 84-PLCC, 100-TQFP, and 100-PQFP package types:

     V_{CCINT} must be between 4.5V and 5.5V while V_{CCIO} can be between 3.0V and 3.6V or 4.5V and 5.5V.
   - ATF15xxAS/ASL CPLDs in 44-PLCC and 44-TQFP package types:

     V_{CC} must be between 4.5V to 5.5V.
   - ATF15xxASV/ASVL CPLDs:

     V_{CC} (V_{CCIO} and V_{CCINT}) must be between 3.0V to 3.6V.
3. The V_{CC} for the devices in the JTAG chain must be properly regulated and filtered.
   - For the ATF15xx CPLDs used in most applications, it is recommended to use one 0.22µF decoupling capacitor for each of the V_{CC}/GND pairs.
4. It is recommended to use a common ground for all of the devices in the JTAG chain and the JTAG interface hardware (i.e. ATDH1150USB ISP Download Cable).
5. It is recommended to avoid long (no more than five devices) JTAG chains.
   - If a long JTAG chain is necessary, buffer the TMS and TCK signals after every fifth device. The use of Schmitt trigger buffer is preferred.
   - Buffers reshape the rise and fall times of the TMS and TCK signals.
   - Need to take into consideration the additional delay incurred by the buffers.
6. It is recommended to use pull-up resistors (4.7KΩ to 10KΩ) for the TMS and TDI signals and pull-down resistor for the TCK signal at the JTAG header to prevent these signals from floating when they are not being driven by the interface hardware.
   - Optional internal pull-ups on TMS and TDI are available for the ATF15xx CPLDs.
7. It is recommended to terminate JTAG signals at the JTAG header.
   - Both active and passive terminations are acceptable; however, passive termination is preferred.
   - It reduces ringing due to long cable/PCB trace lengths.
   - Termination is most critical for TMS and TCK.
8. It is recommended that all of the inputs and I/Os of the devices in the JTAG chain, except the JTAG pins, should be in static state when the ATF15xx CPLDs are being programmed to minimize noise.

9. When using one of the Atmel ATF15xx development/programmer board, power to the board must be turned OFF when the positions of the V_{CC} selection jumpers are being changed.
10. For the ATF15xx CPLDs, JTAG ISP is available when the part is in Pin-controlled Power-down mode or when “low-power” device is asleep.
11. Device state after interruption of ISP:
    - If ISP is interrupted, all I/O pins are **tri-stated** regardless of the state of the Pin-keeper circuits.
    - Prevents partially programmed device from causing bus contention with other devices on circuit board.
12. During ISP programming, all I/O pins are in one of the following conditions:
    - High-impedance state:
        - When a blank/erased device is programmed.
        - When a device is re-programmed with the Pin-keeper circuits disabled.
        - Prevents bus contention with external devices interfacing with the ATF15xx CPLDs on the circuit board.
    - Weakly latched to the previous state:
        - When a programmed device is re-programmed with the Pin-keeper circuits enabled.
        - I/O pins keep previous logic levels prior to ISP.
        - Prevents ISP from affecting the operation of other devices on the system board.
13. The use of multiple JTAG chains on one board is not recommended.
    - Devices may interact between different JTAG chains.
    - Board is functional only when **all** devices in **all** JTAG chains are programmed successfully.
    - If programming fails for at least one device in a chain while other JTAG chains were successfully programmed:
        - Either Atmel or other devices on board can be damaged due to possible bus contention problem for tri-stateable outputs.
        - System board operational state is undefined; and therefore, incorrect functional operation may occur.
14. Inserting active circuits between JTAG header and the JTAG devices in chain is not recommended. If active circuit malfunctions, it may cause programming/verify problems.
15. The use of mixed-voltage device JTAG chains is not recommended.
    - These are JTAG chains with devices that use different V_{CC} voltages and/or interface voltages.
    - Interface voltage levels (V_{IL}, V_{IH}, V_{OL}, V_{OH}) for 5.0V devices might not be compatible with interface voltage levels for 3.0V devices.
16. If ATMISP has problem communicating with the JTAG device hardware chain, try running Self Calibrate or Manually Calibrate to lower the frequencies of the JTAG signals.
17. Make sure the LED on the ATDH1150USB cable is turned on and it’s green before programming starts. Ensure the ISP download cable is able to properly communicate with the ATMISP software.
18. Make sure the proper V_{CC} voltage is applied to the ATDH1150USB cable.
    - The V_{CC} used by the first device in the JTAG chain must be supplied to the ATDH1150USB cable via pin 4 of the 10-pin JTAG header.
    - For ATF15xx CPLDs with separate V_{CCINT} and V_{CCIO}, V_{CCIO} should be used for the ATDH1150USB cable.

5. Ordering Information

Ordering Code	Description
ATF15xx-DK3-U	CPLD Development/Programmer Kit (includes the ATF15xxDK3-SAA44 and ATDH1150USB or ATDH1150USB-K)
ATF15xxDK3-SAA100	100-pin TQFP Socket Adapter Board for DK3 Board
ATF15xxDK3-SAJ44	44-pin PLCC Socket Adapter Board for DK3 Board
ATF15xxDK3-SAJ84	84-pin PLCC Socket Adapter Board for DK3 Board
ATF15xxDK3-SAA44	44-pin TQFP Socket Adapter Board for DK3 Board
ATDH1150USB	Atmel ATF15xx CPLD USB-based JTAG ISP Download Cable

6. Revision History

Doc. Rev.	Date	Comments
A	12/2015	Initial document release.

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