

Arm® Cortex®-M4 32b MCU+FPU, 125 DMIPS, 512KB Flash, 128KB RAM, USB OTG FS, 11 TIMs, 1 ADC, 13 comm. interfaces

Table 7. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/ output pin
I/O structure	FT	5 V tolerant I/O
	TC	Standard 3.3 V I/O
	B	Dedicated BOOT0 pin
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

LEGENDE POUR LES ANNOTATIONS

Les commentaires signalent les broches utilisées.

Lorsqu’une de ces broches est utilisée avec une “fonction alternative”, elle est **surlignée en bleu**

Même broche -Même fonction

Broche différente -Même fonction

Fonction uniquement sur LQFP64

Pin number					Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100						
X	X									-
X	Y									-
-	Z									-

Table 8. STM32F411xC/xE pin definitions

Pin number					Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100						
-	-	-	1	B2	PE2	I/O	FT	-	TRACECLK, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, EVENTOUT	-
-	-	-	2	A1	PE3	I/O	FT	-	TRACED0, EVENTOUT	-
-	-	-	3	B1	PE4	I/O	FT	-	TRACED1, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, EVENTOUT	-
-	-	-	4	C2	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SPI5_MISO, EVENTOUT	-

Table 8. STM32F411xC/xE pin definitions (continued)

Pin number					Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100						
-	-	-	5	D2	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, EVENTOUT	-
-	-	-	-	D3	VSS	S	-	-	-	-
-	-	-	-	C4	VDD	S	-	-	-	-
1	1	B7	6	E2	VBAT	S	-	-	-	-
2	2	D5	7	C1	PC13- ANTI_TAMP	I/O	FT	(2)(3)	-	RTC_AMP1, RTC_OUT, RTC_TS
3	3	C7	8	D1	PC14- OSC32_IN	I/O	FT	(2)(3) (4)	-	OSC32_IN
4	4	C6	9	E1	PC15- OSC32_OUT	I/O	FT	-	-	OSC32_OUT
-	-	-	10	F2	VSS	S	-	-	-	-
-	-	-	11	G2	VDD	S	-	-	-	-
5	5	D7	12	F1	PH0 - OSC_IN	I/O	FT	-	-	OSC_IN
6	6	D6	13	G1	PH1 - OSC_OUT	I/O	FT	-	-	OSC_OUT
7	7	E7	14	H2	NRST	I/O	FT	-	EVENTOUT	-
-	8	-	15	H1	PC0	I/O	FT	-	EVENTOUT	ADC1_10
-	9	-	16	J2	PC1	I/O	FT	-	EVENTOUT	ADC1_11
-	10	-	17	J3	PC2	I/O	FT	-	SPI2_MISO, I2S2ext_SD, EVENTOUT	ADC1_12
-	11	-	18	K2	PC3	I/O	FT	-	SPI2_MOSI/I2S2_SD, EVENTOUT	ADC1_13
-	-	-	19	-	VDD	S	-	-	-	-
8	12	E6	20	J1	VSSA	S	-	-	-	-
-	-	-	-	K1	VREF-	S	-	-	-	-
9	13	F7	21	L1	VREF+	S	-	-	-	-
-	-	-	22	M1	VDDA	S	-	-	-	-

Table 8. STM32F411xC/xE pin definitions (continued)

Pin number					Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100						
10	14	F6	23	L2	PA0-WKUP	I/O	TC	(5)	TIM2_CH1/TIM2_ET, TIM5_CH1, USART2_CTS, EVENTOUT	ADC1_0, WKUP1
11	15	G7	24	M2	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, SPI4_MOSI/I2S4_SD, USART2_RTS, EVENTOUT	ADC1_1
12	16	E5	25	K3	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, I2S2_CKIN, USART2_TX, EVENTOUT	ADC1_2
13	17	E4	26	L3	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, I2S2_MCK, USART2_RX, EVENTOUT	ADC1_3
-	18	-	27	-	VSS	S	-	-	-	-
-	-	-	-	E3	BYPASS_REG	S	-	-	-	-
-	19	-	28	-	VDD	I	FT	-	EVENTOUT	-
14	20	G6	29	M3	PA4	I/O	FT	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT	ADC1_4
15	21	F5	30	K4	PA5	I/O	FT	-	TIM2_CH1/TIM2_ET, SPI1_SCK/I2S1_CK, EVENTOUT	ADC1_5
16	22	F4	31	L4	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, SPI1_MISO, I2S2_MCK, SDIO_CMD, EVENTOUT	ADC1_6
17	23	F3	32	M4	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, SPI1_MOSI/I2S1_SD, EVENTOUT	ADC1_7

Table 8. STM32F411xC/xE pin definitions (continued)

Pin number					Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100						
-	24	-	33	K5	PC4	I/O	FT	-	EVENTOUT	ADC1_14
-	25	-	34	L5	PC5	I/O	FT	-	EVENTOUT	ADC1_15
18	26	G5	35	M5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, SPI5_SCK/I2S5_CK, EVENTOUT	ADC1_8
19	27	G4	36	M6	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, SPI5_NSS/I2S5_WS, EVENTOUT	ADC1_9
20	28	G3	37	L6	PB2	I/O	FT	-	EVENTOUT	BOOT1
-	-	-	38	M7	PE7	I/O	FT	-	TIM1_ETR, EVENTOUT	-
-	-	-	39	L7	PE8	I/O	FT	-	TIM1_CH1N, EVENTOUT	-
-	-	-	40	M8	PE9	I/O	FT	-	TIM1_CH1, EVENTOUT	-
-	-	-	41	L8	PE10	I/O	FT	-	TIM1_CH2N, EVENTOUT	-
-	-	-	42	M9	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS/I2S4_WS, SPI5_NSS/I2S5_WS, EVENTOUT	-
-	-	-	43	L9	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK/I2S4_CK, SPI5_SCK/I2S5_CK, EVENTOUT	-
-	-	-	44	M10	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, SPI5_MISO, EVENTOUT	-
-	-	-	45	M11	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI/I2S4_SD, SPI5_MOSI/I2S5_SD, EVENTOUT	-
-	-	-	46	M12	PE15	I/O	FT	-	TIM1_BKIN, EVENTOUT	-

Table 8. STM32F411xC/xE pin definitions (continued)

Pin number					Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100						
21	29	E3	47	L10	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, I2S3_MCK, SDIO_D7, EVENTOUT	-
-	-	-	-	K9	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, I2S2_CKIN, EVENTOUT	-
22	30	G2	48	L11	VCAP_1	S	-	-	-	-
23	31	D3	49	F12	VSS	S	-	-	-	-
24	32	F2	50	G12	VDD	S	-	-	-	-
25	33	E2	51	L12	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, SPI4_NSS/I2S4_WS, SPI3_SCK/I2S3_CK, EVENTOUT	-
26	34	G1	52	K12	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, SPI4_SCK/I2S4_CK, EVENTOUT	-
27	35	F1	53	K11	PB14	I/O	FT	-	TIM1_CH2N, SPI2_MISO, I2S2ext_SD, SDIO_D6, EVENTOUT	-
28	36	E1	54	K10	PB15	I/O	FT	-	RTC_50Hz, TIM1_CH3N, SPI2_MOSI/I2S2_SD, SDIO_CK, EVENTOUT	RTC_REFIN
-	-	-	55	-	PD8	I/O	FT	-	-	-
-	-	-	56	K8	PD9	I/O	FT	-	-	-
-	-	-	57	J12	PD10	I/O	FT	-	-	-
-	-	-	58	J11	PD11	I/O	FT	-	-	-
-	-	-	59	J10	PD12	I/O	FT	-	TIM4_CH1, EVENTOUT	-

Table 8. STM32F411xC/xE pin definitions (continued)

Pin number					Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100						
-	-	-	60	H12	PD13	I/O	FT	-	TIM4_CH2, EVENTOUT	-
-	-	-	61	H11	PD14	I/O	FT	-	TIM4_CH3, EVENTOUT	-
-	-	-	62	H10	PD15	I/O	FT	-	TIM4_CH4, EVENTOUT	-
-	37	-	63	E12	PC6	I/O	FT	-	TIM3_CH1, I2S2_MCK, USART6_TX, SDIO_D6, EVENTOUT	-
-	38	-	64	E11	PC7	I/O	FT	-	TIM3_CH2, SPI2_SCK/I2S2_CK, I2S3_MCK, USART6_RX, SDIO_D7, EVENTOUT	-
-	39	-	65	E10	PC8	I/O	FT	-	TIM3_CH3, USART6_CK, SDIO_D0, EVENTOUT	-
-	40	-	66	D12	PC9	I/O	FT	-	MCO_2, TIM3_CH4, I2C3_SDA, I2S2_CKIN, SDIO_D1, EVENTOUT	-
29	41	D1	67	D11	PA8	I/O	FT	-	MCO_1, TIM1_CH1, I2C3_SCL, USART1_CK, USB_FS_SOF, SDIO_D1, EVENTOUT	-
30	42	D2	68	D10	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, USART1_TX, USB_FS_VBUS, SDIO_D2, EVENTOUT	OTG_FS_VBUS

Table 8. STM32F411xC/xE pin definitions (continued)

Pin number					Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100						
31	43	C2	69	C12	PA10	I/O	FT	-	TIM1_CH3, SPI5_MOSI/I2S5_SD, USART1_RX, USB_FS_ID, EVENTOUT	-
32	44	C1	70	B12	PA11	I/O	FT	-	TIM1_CH4, SPI4_MISO, USART1_CTS, USART6_TX, USB_FS_DM, EVENTOUT	-
33	45	C3	71	A12	PA12	I/O	FT	-	TIM1_ETR, SPI5_MISO, USART1_RTS, USART6_RX, USB_FS_DP, EVENTOUT	-
34	46	B3	72	A11	PA13	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
-	-	-	73	C11	VCAP_2	S	-	-	-	-
35	47	B1	74	F11	VSS	S	-	-	-	-
36	48	B2	75	G11	VDD	S	-	-	-	-
37	49	A1	76	A10	PA14	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
38	50	A2	77	A9	PA15	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART1_TX, EVENTOUT	-
-	51	-	78	B11	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, SDIO_D2, EVENTOUT	-
-	52	-	79	C10	PC11	I/O	FT	-	I2S3ext_SD, SPI3_MISO, SDIO_D3, EVENTOUT	-
-	53	-	80	B10	PC12	I/O	FT	-	SPI3_MOSI/I2S3_SD, SDIO_CK, EVENTOUT	-

Table 8. STM32F411xC/xE pin definitions (continued)

Pin number					Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100						
-	-	-	81	C9	PD0	I/O	FT	-	EVENTOUT	-
-	-	-	82	B9	PD1	I/O	FT	-	EVENTOUT	-
-	54	-	83	C8	PD2	I/O	FT	-	TIM3_ETR, SDIO_CMD, EVENTOUT	-
-	-	-	84	B8	PD3	I/O	FT	-	SPI2_SCK/I2S2_CK, USART2_CTS, EVENTOUT	-
-	-	-	85	B7	PD4	I/O	FT	-	USART2_RTS, EVENTOUT	-
-	-	-	86	A6	PD5	I/O	FT	-	USART2_TX, EVENTOUT	-
-	-	-	87	B6	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, USART2_RX, EVENTOUT	-
-	-	-	88	A5	PD7	I/O	FT	-	USART2_CK, EVENTOUT	-
39	55	A3	89	A8	PB3	I/O	FT	-	JTDO-SWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, I2C2_SDA, EVENTOUT	-
40	56	A4	90	A7	PB4	I/O	FT	-	JTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, I2C3_SDA, SDIO_D0, EVENTOUT	-
41	57	B4	91	C5	PB5	I/O	TC	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, SDIO_D3, EVENTOUT	-
42	58	C4	92	B5	PB6	I/O	FT	-	TIM4_CH1, I2C1_SCL, USART1_TX, EVENTOUT	-

Table 8. STM32F411xC/xE pin definitions (continued)

Pin number					Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48	LQFP64	WLCSP49	LQFP100	UFBGA100						
43	59	D4	93	B4	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, SDIO_D0, EVENTOUT	-
44	60	A5	94	A4	BOOT0	I	B	-	-	VPP
45	61	B5	95	A3	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, SPI5_MOSI/I2S5_SD, I2C3_SDA, SDIO_D4, EVENTOUT	-
46	62	C5	96	B3	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, I2C2_SDA, SDIO_D5, EVENTOUT	-
-	-	-	97	C3	PE0	I/O	FT	-	TIM4_ETR, EVENTOUT	-
-	-	-	98	A2	PE1	I/O	FT	-	EVENTOUT	-
47	63	A6	99	-	VSS	S	-	-	-	-
-	-	B6	-	H3	PDR_ON	I	FT	-	-	-
48	64	A7	100	-	VDD	S	-	-	-	-

- Function availability depends on the chosen device.
- PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
 - The speed should not exceed 2 MHz with a maximum load of 30 pF.
 - These I/Os must not be used as a current source (e.g. to drive an LED).
- Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F411xx reference manual.
- FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
- If the device is delivered in an UFBGA100 and the BYPASS_REG pin is set to VDD (Regulator off/internal reset ON mode), then PA0 is used as an internal Reset (active low)